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AN10015_2

Interfacing ISP1161x to Fujitsu® SPARClite® RISC Processor

January 2003

Application Note

Rev. 2.2

Revision History:

Rev	Date	Descriptions	Author
2.2	Jan 2003	Updated the following sections • Section 1 • Section 2 • Section 4 • Section 6 • Removed the section on suspend and resume.	Jason Ong
2.1	Sep2002	• Changed to the latest Philips document template • Changed ISP1161 to ISP1161x • Changed the file name from INTFG_1161_TO_SPARCLITE-02.pdf to AN10015-01.pdf.	Kunzang Dolma
2.0	Oct, 2001	• Updated schematic to reflect use of ES2 • Updated data to reflect latest ISP1161x datasheet • Updated to latest Philips document template	Yuk-lin Ong
1.0	Jan 2001	First release	Socol Constantin

Note: ISP1161x denotes any Philips USB single-chip host and device controller whose name starts with 'ISP1161', this includes ISP1161A, ISP1161A1 and any future derivatives.

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FIGURES

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1. Overview

The unique design of the Philips ISP1161x allows it to be used both as a Host Controller (with two downstream facing ports) and a Device Controller (with one upstream facing port). These ports may be independently accessed, enabling simultaneous connection as a Host Controller and a Device Controller.

When ISP1161x is integrated into a personal digital assistant (PDA) or handheld personal computer (HPC), it is usually connected to the external bus interface of a Reduced Instruction Set Computer (RISC) processor. This application note presents some of the important issues in such a design, using a concrete example of the Fujitsu SPARClite RISC.

2. ISP1161x Processor Interface Signals

ISP1161x's processor bus interface is designed for a simple direct connection with a RISC processor. The data transfer can be done in the Programmed I/O (PIO) or direct memory access (DMA) mode. The estimated maximum data transfer rate on ISP1161x's generic processor bus is approximately 15 Mbyte/s. This is based on an ISP1161x internal clock frequency value of 48 MHz. To achieve the maximum data transfer rate on the host processor bus, ISP1161x contains a ping pong structured RAM that allows alternative access from the RISC processor or from the internal Host Controller and the Device Controller. The ping pong memory is separately allocated for the Host Controller and the Device Controller. The Host Controller uses 2 kbytes of the ping memory and 2 kbytes of the pong memory in its allocated memory. The Device Controller uses 1.5 kbytes for each of the ping and the pong memory in its own memory.

The main ISP1161x signals to consider for connecting to a Fujitsu SPARClite RISC processor are:

- A 16-bit data bus: (D[15:0]) for ISP1161x, which is "little endian" compatible.
- Two address lines (A0 and A1) necessary for complete addressing of the ISP1161x internal registers:
  - **A0 = 0 and A1 = 0**—Selects the Data Port of the Host Controller
  - **A0 = 1 and A1 = 0**—Selects the Command Port of the Host Controller
  - **A0 = 0 and A1 = 1**—Selects the Data Port of the Device Controller
  - **A0 = 1 and A1 = 1**—Selects the Command Port of the Device Controller.
- One $\overline{\text{CS}}$ line used to select ISP1161x in a certain address range of the host system. This input signal is active LOW.
- $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are common read and write signals. These signals are active LOW.
- Two DMA channel standard control lines: DREQ1, DREQ2, DACK1, DACK2 and EOT (one channel is used by the Host Controller, and the other channel is used by the Device Controller). Since the SPARClite processor does not contain a DMA controller, these signals will not be used in a minimal hardware implementation.
- Two interrupt lines:
  - INT1 (used by the Host Controller), and
  - INT2 (used by the Device Controller).

  Both have programmable level or edge, and polarity (active HIGH or LOW).
- The CLKOUT signal has a maximum value of 48 MHz.
- The $\overline{\text{RESET}}$ signal is active LOW.

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3. Fujitsu SPARClite

The SPARClite processor is a part of the 32-bit RISC Fujitsu family, whose maximum CPU frequency is 120 MHz and maximum bus frequency is 40 MHz.

The external bus interface of the SPARClite processor is a non-multiplexed address and data bus. It has a big-endian architecture. An internal programmable Chip Select logic and an on-chip address decoder allow easy interfacing to EPROM, DRAM (EDO/FPM), UART, or general ASIC without additional glue logic. The integrated DRAM controller can generate all signals necessary providing a direct interface to different types of memory; FPM and EDO DRAMS. The address decoder of the SPARClite processor can generate six programmable Chip Select signals. One of the CS0–CS5 signals will be asserted when the selected address matches the value programmed in the *Address Range Specifier Register*. The *Address Mask Register* is used to mask certain bits of the address.

To select the properties of each area, set certain values in the internal control registers:

- Bus size: 8, 16 or 32 bits can be independently set for each area, and is determined by the value of the *Bus Width/Cacheable Register* of the SPARClite processor.
- Number of wait cycles: can be independently set for each selected area by setting the *Wait States Specifier Register* of SPARClite.
- Setting the type of space: SRAM, DRAM and EPROM. The SPARClite processor will generate the necessary signals to control any of these types of memory.

Each addressed area of the SPARClite processor can be used only in the big endian mode. For correct data alignment, matching data width and endian is necessary. In the design phase of a system using SPARClite and ISP1161x, care must be taken during schematics and software development because the ISP1161x connection requires a 16-bit or little endian configuration of the selected memory area.

4. Considerations in Timing Diagrams and WAIT States

The following is a short study of the timing diagrams of ISP1161x.

According to the ISP1161x datasheet specifications, a read cycle requires the following main timing parameters (the requirements of the write cycle are similar):

- t_{RL} = 33 ns ($\overline{RD}$ LOW pulse width—minimal value required by ISP1161x),
- t_{RHRL} = 110 ns ($\overline{RD}$ HIGH to next $\overline{RD}$ LOW—minimal value required by ISP1161x) and
- t_{RHDZ} = 3 ns ($\overline{RD}$ hold time, minimal value that can be expected from ISP1161x).
- t_{RC} = 143 ns (will result as a sum of t_{RL} and t_{RHRL})
- t_{SHSL} = 300 ns (first $\overline{RD}$/$\overline{WR}$ after command).

For a detailed analysis of a timing diagram, consider the access of an ISP1161x internal register (for example, the Control Register of the Host Controller). It requires two phases: writing the address (index) of the selected register into the Command Port; then only data transfer access (RD/WR) may take place.

The timing diagram in Figure 4-1 describes the two phases of accessing ISP1161x:

- The first phase is accessing the Command (control) Port of ISP1161x, to write the address (index) of the data port that will be accessed. In this phase, $\overline{CS}$ is active. The data lines D[15:0] contain the desired address. The $\overline{WR}$ pulse will be activated and will latch the data. Note the value of t_{SHSL} that represents the minimum time required between occurrence of the first phase and the second phase. As an example of the Host Controller "Control Register", a value of 01H will be transferred during a $\overline{RD}$ operation and 81H during a $\overline{WR}$ operation.
- The second phase consists of the access (read or write) to the data port selected by the address latched in the previous phase. Two timing diagrams are combined again in this second phase: one for the read access and one for the write access. A series of $\overline{RD}$ and $\overline{WR}$ pulses are shown in the diagram to define

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the timing requirements between two consecutive accesses to ISP1161x: t_{RHRL}, t_{WHWL}, t_{RC}, t_{WC}, t_{RLDV}, as specified in the datasheet.

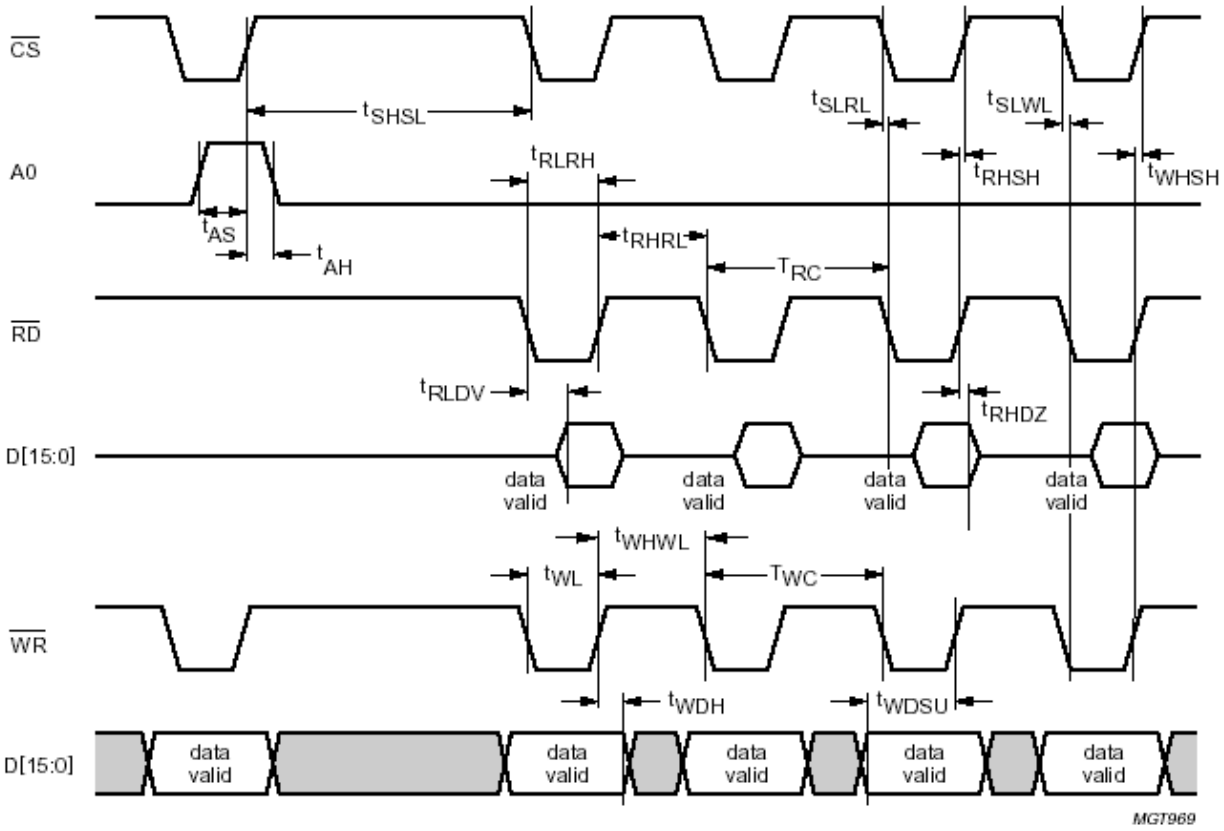

Figure 4-1: Programmed Interface Timing (16-bit Read/Write)

When the ISP1161x connection area is defined as SRAM, ISP1161x will operate correctly for a bus clock CKIO = 33 MHz. Timing measurements show that inserting wait-states in the standard bus cycles of SPARClite is not necessary. Nevertheless, we will describe wait-state insertion, to cater for cases when faster bus cycles are used for accessing ISP1161x.

Wait states insertion may be generally achieved using two solutions: hardware or software implementation. Both solutions will delay the rising edge of $\overline{RD}$ or $\overline{WR}$ to the next CKIO cycle and will determine an elongation of the $\overline{RD}$ or $\overline{WR}$ LOW pulse that can be calculated as:

t_w = W x T(CKIO); where: (W) is the number of wait states desired or selected.

T(CKIO) is the cycle length of CKIO.

Note: the value of t_{RHRL} will not be modified by the number of wait states inserted by any of the solutions mentioned earlier. The value of this parameter must be calculated and correctly adjusted according to the number and length of instructions executed by the SPARClite processor between two successive accesses to ISP1161x. The "software solution" for wait-state insertion in a bus cycle is simple and is preferred in a minimal configuration, if additional wait states are necessary.

5. Using Interrupts

ISP1161x generates two interrupts on the INT1 and INT2 pins, allocated for the Host Controller and the Device Controller, respectively. These interrupts occur depending on the setting of the interrupt registers.

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Connection of the INT1 and INT2 signals can be done directly to any available IRQ signal of the SPARClite processor. Both INT1 and INT2 of the ISP1161x are programmable as active on level or edge and HIGH or LOW, as specified in the *HcHardwareConfiguration* Register and *DcHardwareConfiguration* Register of the Host Controller and Device Controller, respectively.

6. Schematic Diagram

The schematic diagram on the following page shows the connection of the ISP1161x to a Fujitsu SPARClite processor in a minimal hardware configuration. For a more detailed description of connection of the ISP1161x to a RISC processor and a study of each category of signals and timing diagrams, refer to the application note *Interfacing ISP1161x to Hitachi SH7709 RISC Processor*.

In this configuration, the ISP1161x is simply selected by CS5# that is asserted according to the values programmed in the *Address Range Specifier Register* and the *Address Mask Register*.

To correctly access the ISP1161x, it is assumed that area 5 is programmed for the SRAM memory type for 16-bit accesses. Data lines D[15:0] of the SPARClite processor will be used in this configuration, and pull-up resistors must be connected to the data bus lines that are not used (D[31:16]); according to the SPARClite datasheet specifications. In this configuration, the $\overline{RD}$ input signal of the ISP1161x is generated by negating the $\overline{RD}/\overline{WR}$ signal generated by the SPARClite processor. Therefore, the $\overline{RD}$ input signal of the ISP1161x will be active most of the time as the SPARClite $\overline{RD}/\overline{WR}$ signal is HIGH during a read or idle cycle. This will not create any conflicts on the system data bus as the ISP1161x will enable its internal output buffers only when $\overline{CS}$ is also active in the same time.

Interrupts INT1 and INT2 are arbitrarily connected to IRQ8 and IRQ9 lines, respectively, of the SPARClite processor. The interrupt controller of the Fujitsu SPARClite processor allows independent setting of the interrupt trigger mode for each input, by programming its *Trigger Mode 0 and 1 Registers*. The ISP1161x also allows programming of polarity (LOW/HIGH) and the signaling mode (level or pulse) for both generated interrupts INT1 and INT2, by correctly setting the bits of the *HcHardwareConfiguration* and *DcHardwareConfiguration* registers of the Host Controller and Device Controller, respectively.

Input signals $\overline{H\_OC1}$ and $\overline{H\_OC2}$ are used by the ISP1161x to detect an overcurrent on the downstream ports. Since separate overcurrent detection and protection circuits are implemented for each downstream port in the ISP1161x, detection of an overcurrent on a downstream port will have power turned off at that port only. Connecting the voltages of the two downstream ports VBUS_DN1 and VBUS_DN2 to $\overline{H\_OC1}$ and $\overline{H\_OC2}$ pins enables current value to be detected by sensing the voltage drop on Q1 and Q2 that are MOS transistors with very low switch-on resistance Rds(on). Selection between Q1 and Q2 depends on the desired maximum current value and this determines the value of Rds(on). For example, if the allowed maximum current is about 0.5 A, a voltage drop of 75 mV will trigger the overcurrent circuitry and Rds(on) of approximately 150 MΩ will result. Connecting the ISP1161x input pins $\overline{H\_OC1}$ and $\overline{H\_OC2}$ to +5 V will disable the internal overcurrent protection of the ISP1161x. You can opt for an external overcurrent protection circuit.

The number of downstream ports is determined by the setting of the NDP_SEL input signal of the ISP1161x. In a minimal hardware configuration, you can use a simple jumper option to set one or two downstream ports.

Detection of a connection on the upstream port is achieved by connecting VBUS_UP to pin D_VBUS of the ISP1161x. R12 and C20 will act as a low-pass filter that eliminates the possibility of sensing false voltage drop because of load current variations or noise on VBUS_UP. It is recommended, if possible, to implement a hybrid power solution, by using VBUS_UP to power the ISP1161x and an external power source for the rest of the system.

The GoodLink™ ($\overline{GL}$) output signal indicates (using an LED) the status of the USB device and helps in troubleshooting the USB connection.

The $\overline{RESET}$ input signal of the ISP1161x is connected to the RESET# input signal of the SPARCLITE processor and both are connected to the system RESET generation circuitry.

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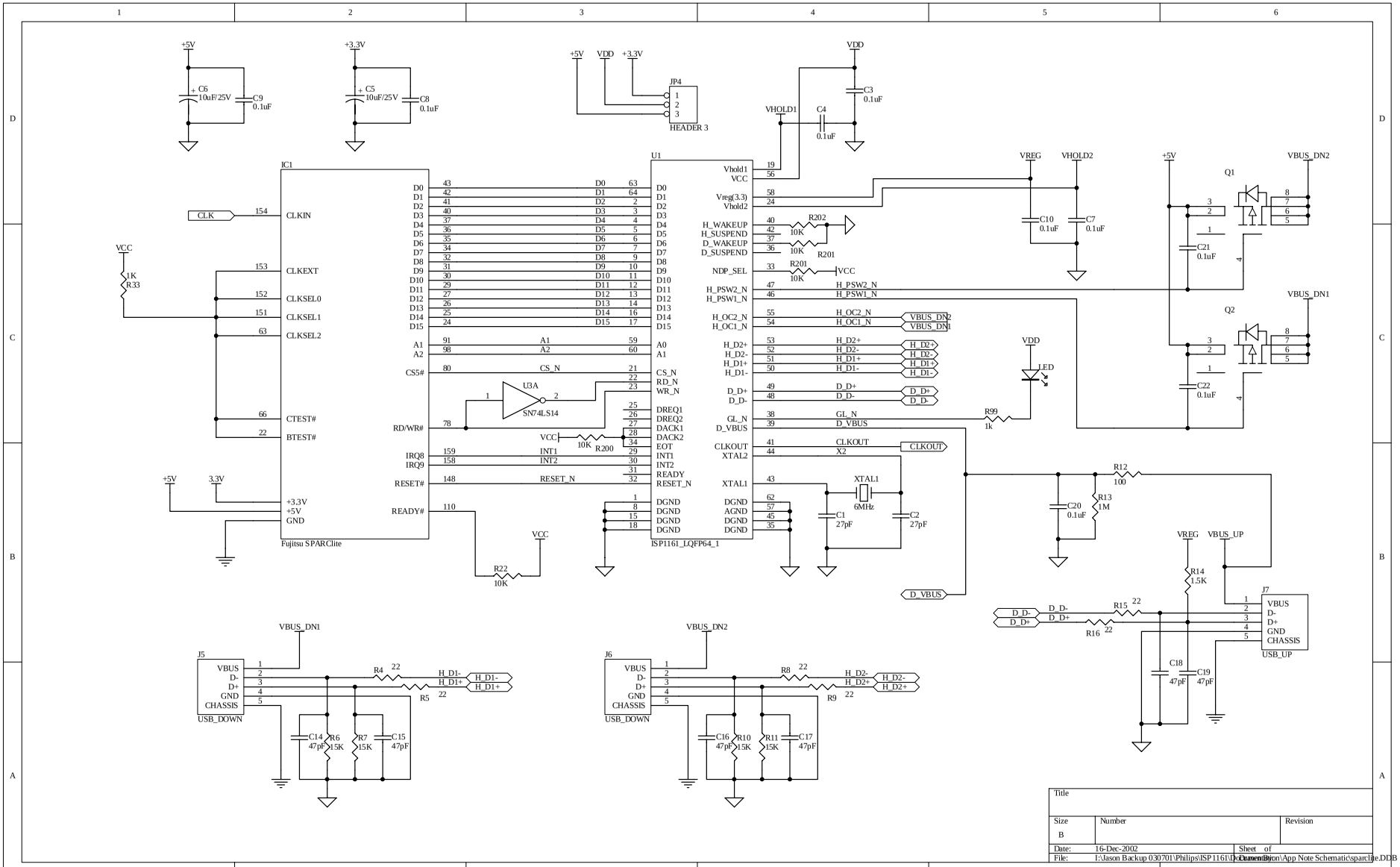

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7. References

- *Universal Serial Bus Specification Rev. 2.0*
- *ISP1161A1 Full-speed Universal Serial Bus single-chip host and device controller* datasheet
- *ISP1161A Full-speed Universal Serial Bus single-chip host and device controller* datasheet
- *ISP1161 Full-speed Universal Serial Bus single-chip host and device controller* datasheet
- *Interfacing ISP1161x to Hitachi SH7709 RISC Processor* application note.

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